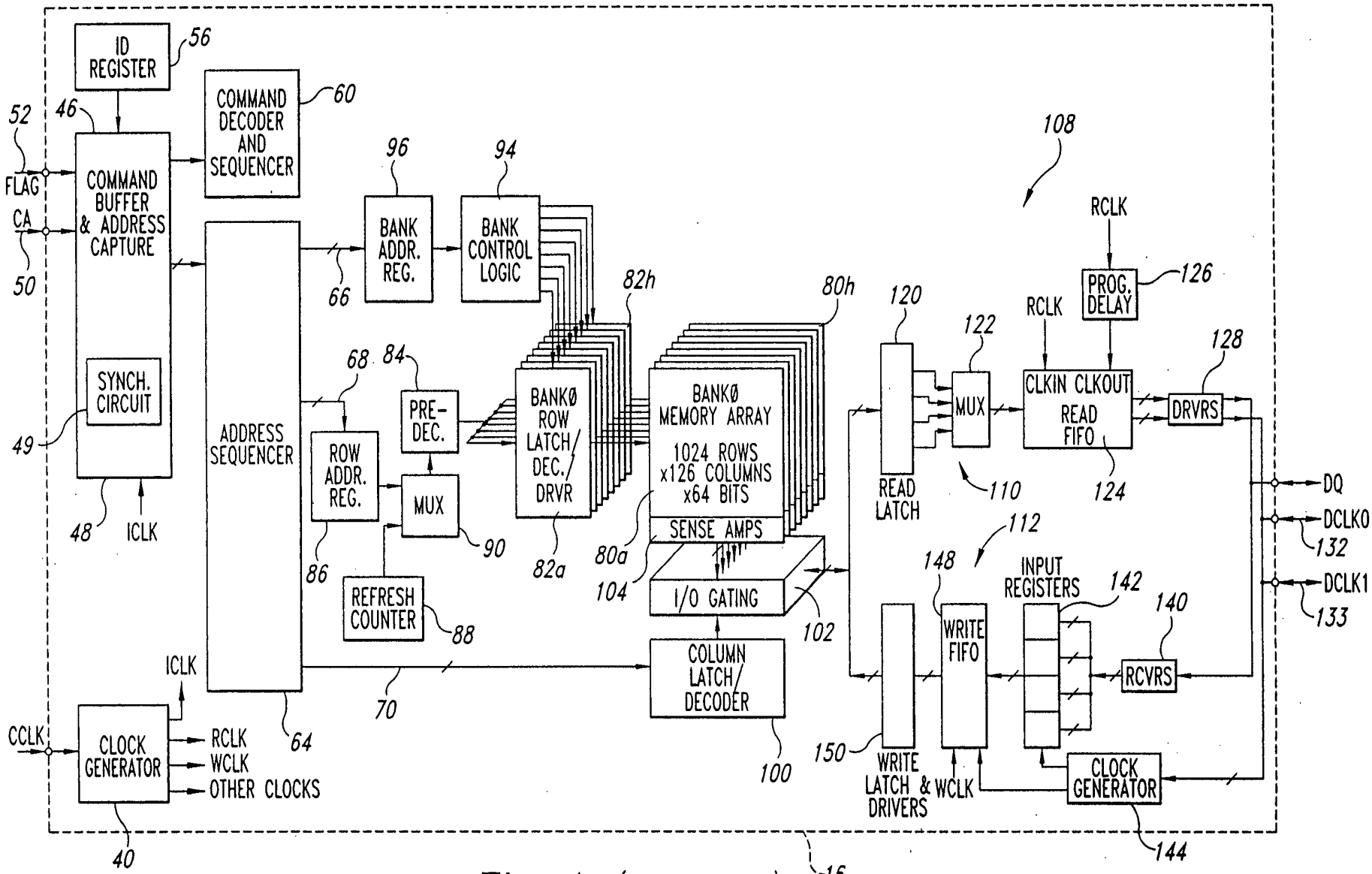


Fig. 1 (PRIOR ART)

	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
PW_1	ID6	ID5	ID4	ID3	ID2	ID1	ID0	CMD5	CMD4	CMD3
PW_2	CMD2	CMD1	CMD0	BNK2	BNK1	BNK0	ROW9	ROW8	ROW7	ROW6
PW_3	ROW5	ROW4	ROW3	ROW2	ROW1	ROW0	0	0	0	0
PW_4	0	0	0	COL6	COL5	COL4	COL3	COL2	COL1	COL0

CA<0:39>

ID6-ID0 = DEVICE ID VALUE
CMD5-CMD0 = COMMAND CODE
BNK2-BNK0 = BANK ADDRESS

ROW9-ROW0 = ROW ADDRESS
COL6-COL0 = COLUMN ADDRESS
0 = UNUSED

Fig. 2
(PRIOR ART)

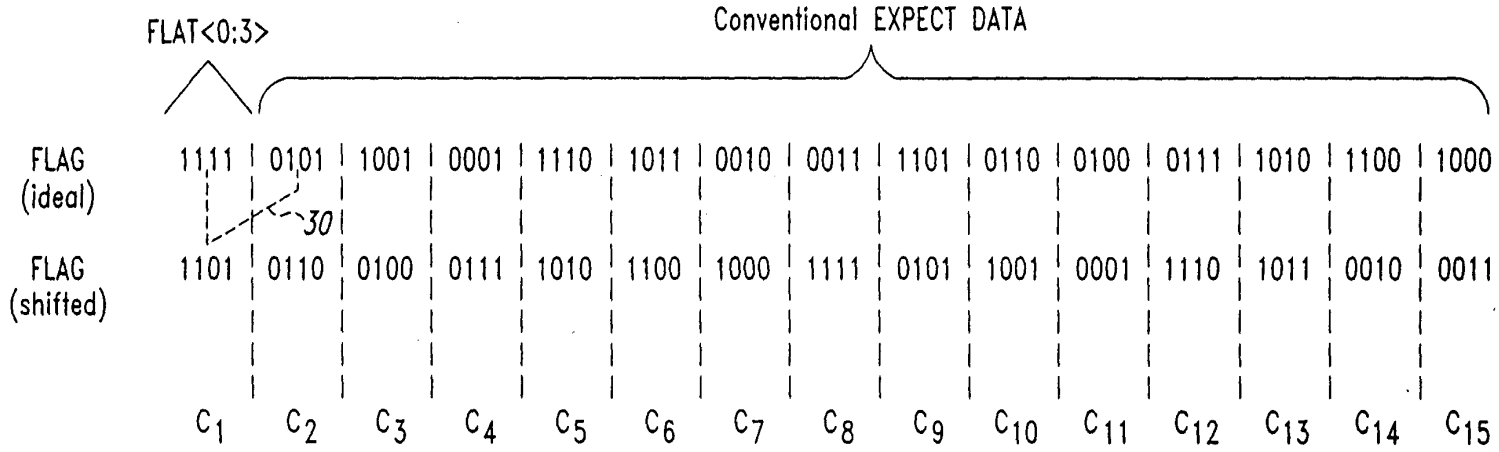


Fig. 3
(PRIOR ART)

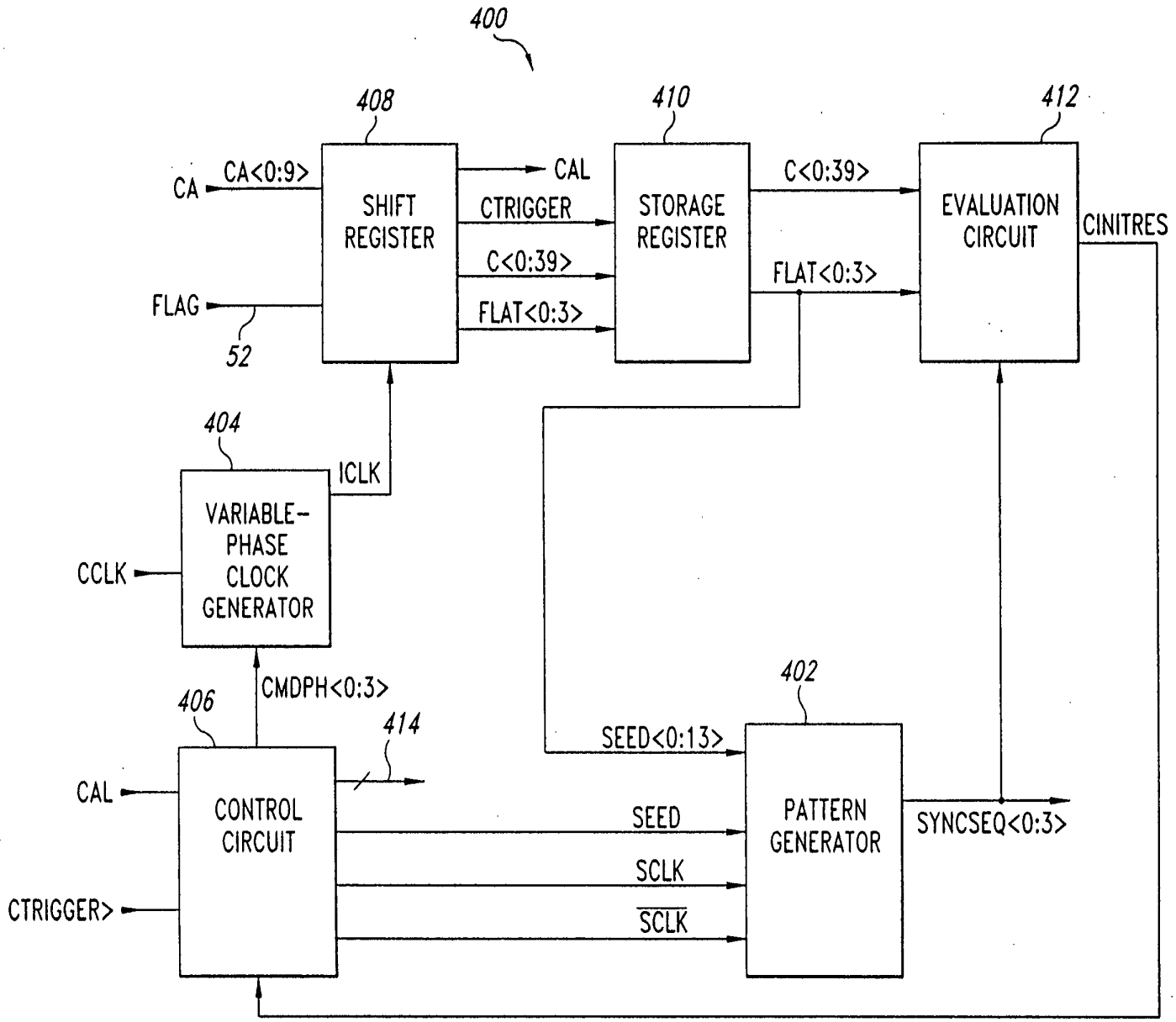

400
408
410
412
CA
CA<0:9>
SHIFT REGISTER
CAL
CTRIGGER
C<0:39>
FLAT<0:3>
STORAGE REGISTER
C<0:39>
FLAT<0:3>
EVALUATION CIRCUIT
CINITRES
FLAG
52
404
ICLK
VARIABLE-PHASE CLOCK GENERATOR
CCLK
CMDPH<0:3>
406
414
402
SEED<0:13>
CAL
CONTROL CIRCUIT
SEED
SCLK
SCLK
PATTERN GENERATOR
SYNCSEQ<0:3>
CTRIGGER>

Fig. 4

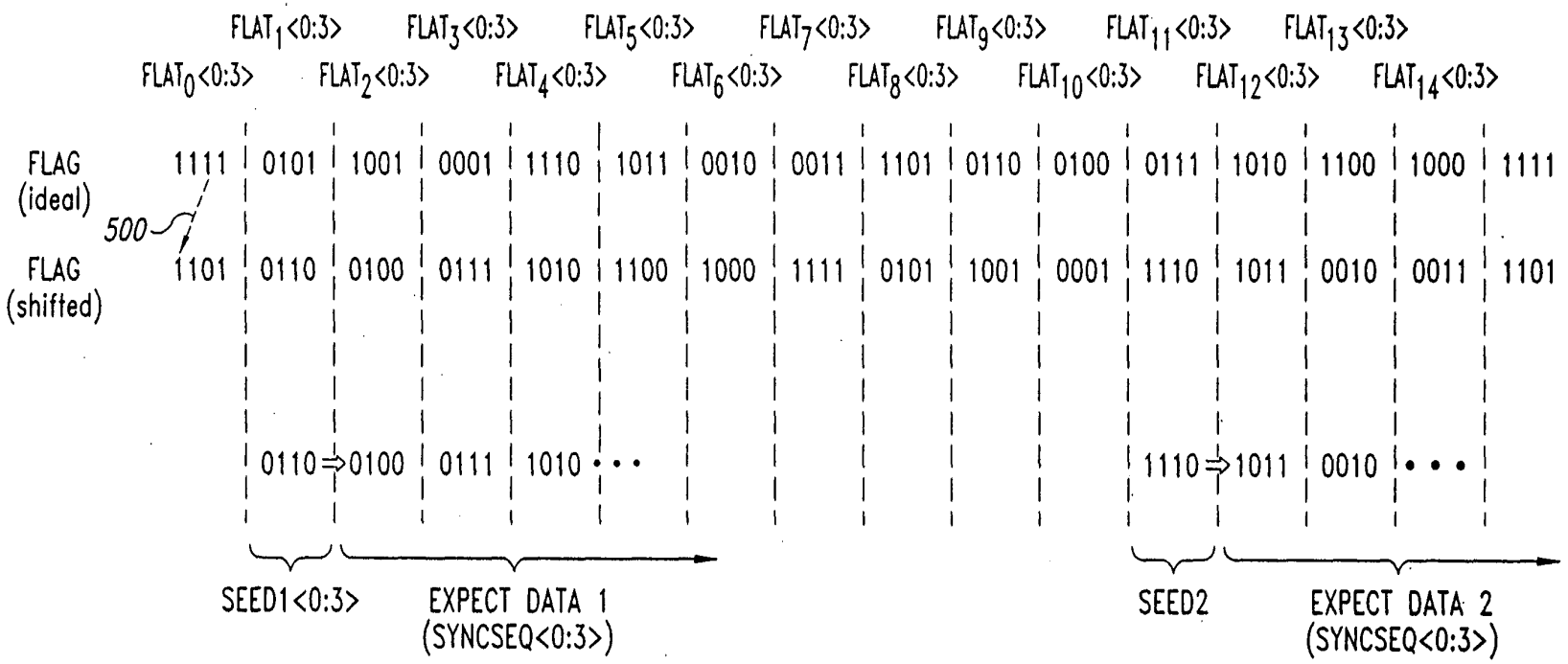
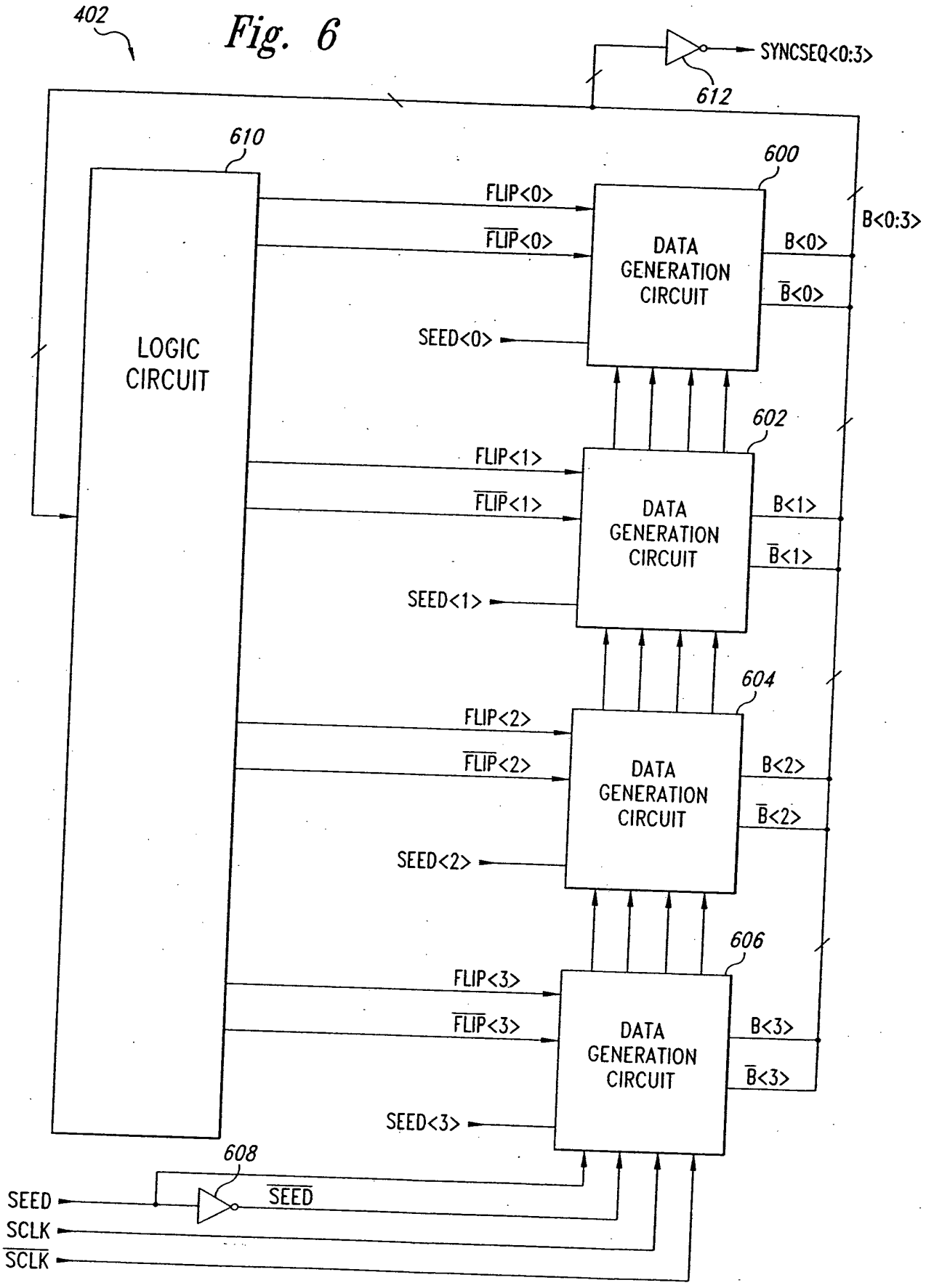

FLAT1<0:3>
FLAT3<0:3>
FLAT5<0:3>
FLAT7<0:3>
FLAT9<0:3>
FLAT11<0:3>
FLAT13<0:3>
FLAT0<0:3>
FLAT2<0:3>
FLAT4<0:3>
FLAT6<0:3>
FLAT8<0:3>
FLAT10<0:3>
FLAT12<0:3>
FLAT14<0:3>
FLAG (ideal)
500
FLAG (shifted)
1111 0101 1001 0001 1110 1011 0010 0011 1101 0110 0100 0111 1010 1100 1000 1111
1101 0110 0100 0111 1010 1100 1000 1111 0101 1001 0001 1110 1011 0010 0011 1101
0110⇒0100 0111 1010 • • •
1110⇒1011 0010 • • •
SEED1<0:3>
EXPECT DATA 1 (SYNCSEQ<0:3>)
SEED2
EXPECT DATA 2 (SYNCSEQ<0:3>)

Fig. 5

Fig. 6


402
SYNCSEQ<0:3>
612
610
600
LOGIC CIRCUIT
FLIP<0>
FLIP<0>
SEED<0>
DATA GENERATION CIRCUIT
B<0>
B<0>
B<0:3>
602
FLIP<1>
FLIP<1>
SEED<1>
DATA GENERATION CIRCUIT
B<1>
B<1>
604
FLIP<2>
FLIP<2>
SEED<2>
DATA GENERATION CIRCUIT
B<2>
B<2>
606
FLIP<3>
FLIP<3>
SEED<3>
DATA GENERATION CIRCUIT
B<3>
B<3>
608
SEED
SEED
SCLK
SCLK

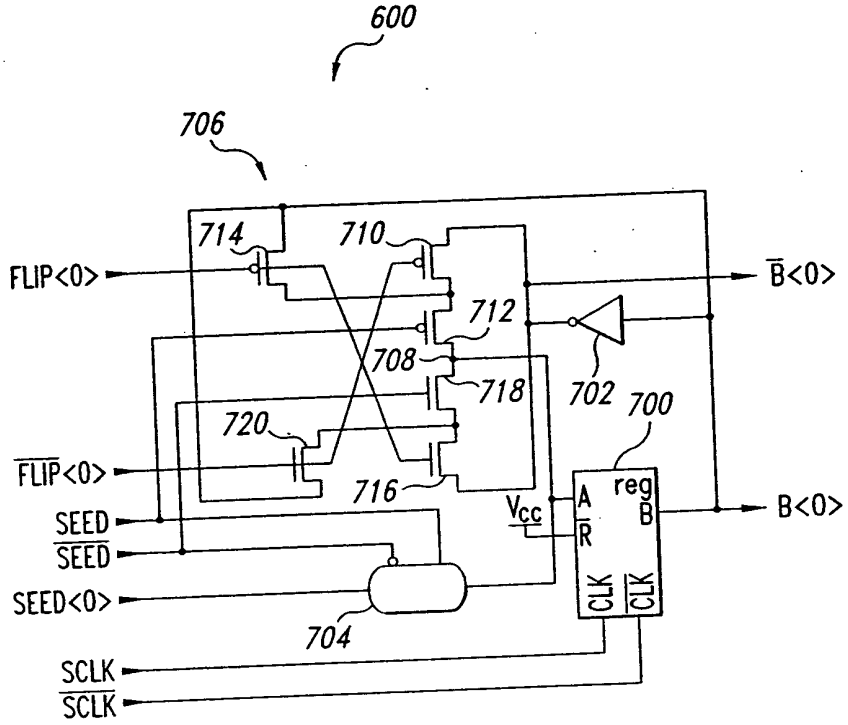

600
706
714
710
FLIP<0>
$\overline{B}$<0>
712
708
718
702
700
720
$\overline{FLIP}$<0>
716
V_{cc}
A
reg
B
R
B<0>
SEED
$\overline{SEED}$
SEED<0>
CLK
$\overline{CLK}$
704
SCLK
$\overline{SCLK}$

Fig. 7

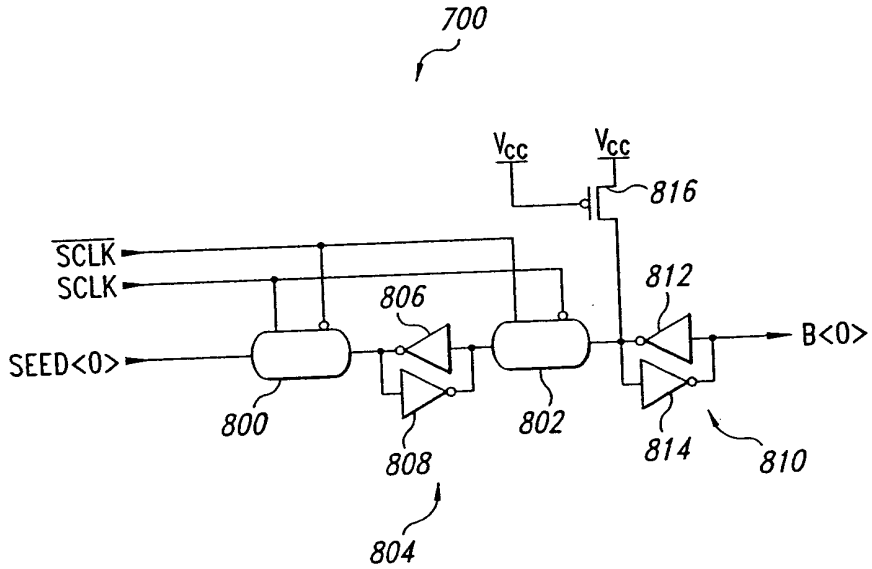

700
V_{cc}
V_{cc}
816
$\overline{SCLK}$
SCLK
806
812
B<0>
SEED<0>
800
802
808
814
810
804

Fig. 8

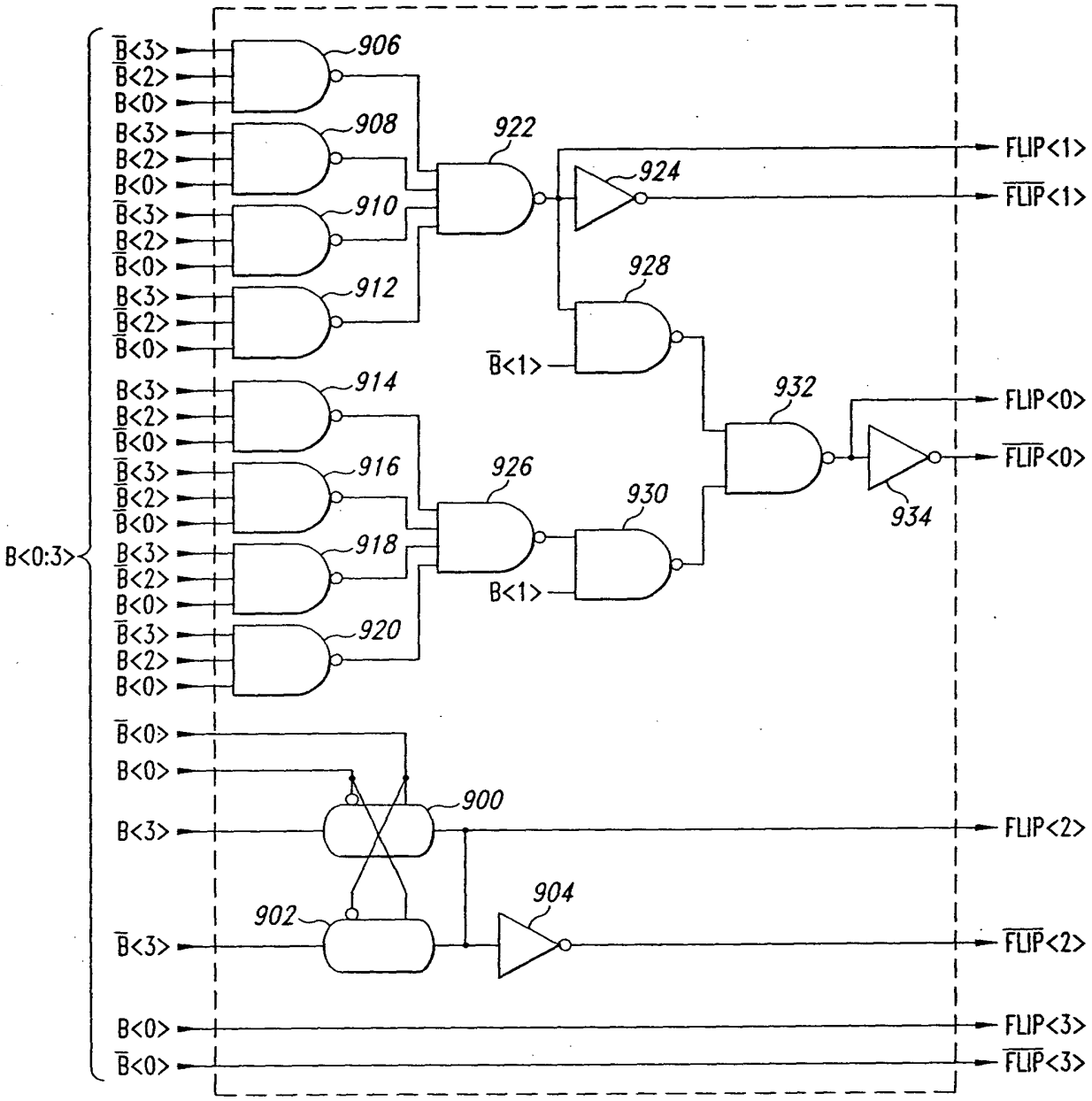

B<0:3>
B<3>
B<2>
B<0>
906
908
910
912
914
916
918
920
922
924
926
928
930
932
934
B<1>
900
902
904
FLIP<1>
FLIP<0>
FLIP<2>
FLIP<3>

Fig. 9

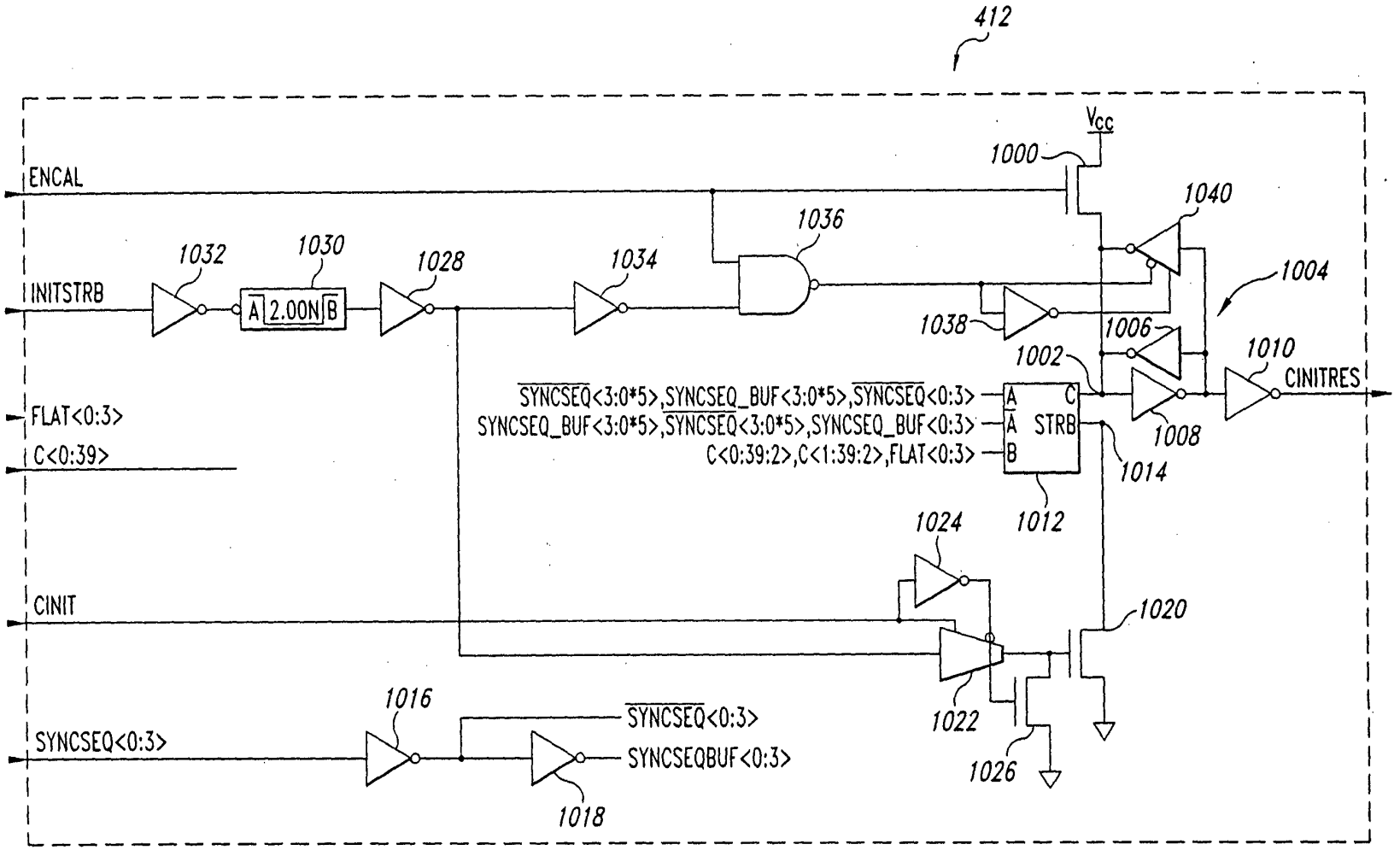
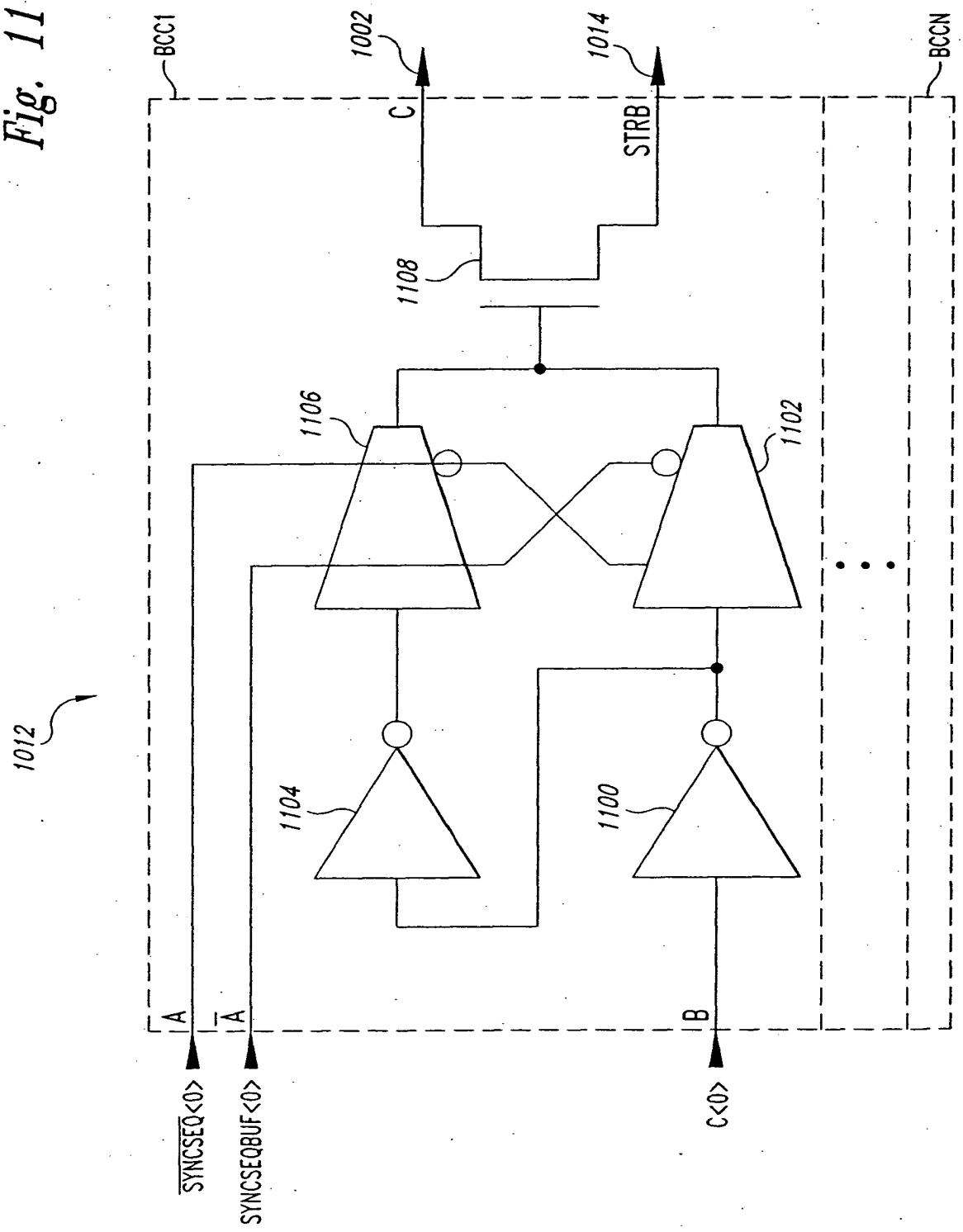

412
ENCAL
INITSTRB
FLAT<0:3>
C<0:39>
CINIT
SYNCSEQ<0:3>
A 2.00N B
SYNCSEQ<3:0*5>,SYNCSEQ_BUF<3:0*5>,SYNCSEQ<0:3>
SYNCSEQ_BUF<3:0*5>,SYNCSEQ<3:0*5>,SYNCSEQ_BUF<0:3>
C<0:39:2>,C<1:39:2>,FLAT<0:3>
A
A
B
C
STRB
SYNCSEQ<0:3>
SYNCSEQBUF<0:3>
Vcc
CINITRES
1000
1002
1004
1006
1008
1010
1012
1014
1016
1018
1020
1022
1024
1026
1028
1030
1032
1034
1036
1038
1040

Fig. 10

Fig. 11


1012
BCC1
1002
1014
BCCN
C
STRB
1108
1106
1102
1104
1100
A
$\overline{A}$
B
$\overline{SYNCSEQ}$<0>
SYNCSEQBUF<0>
C<0>

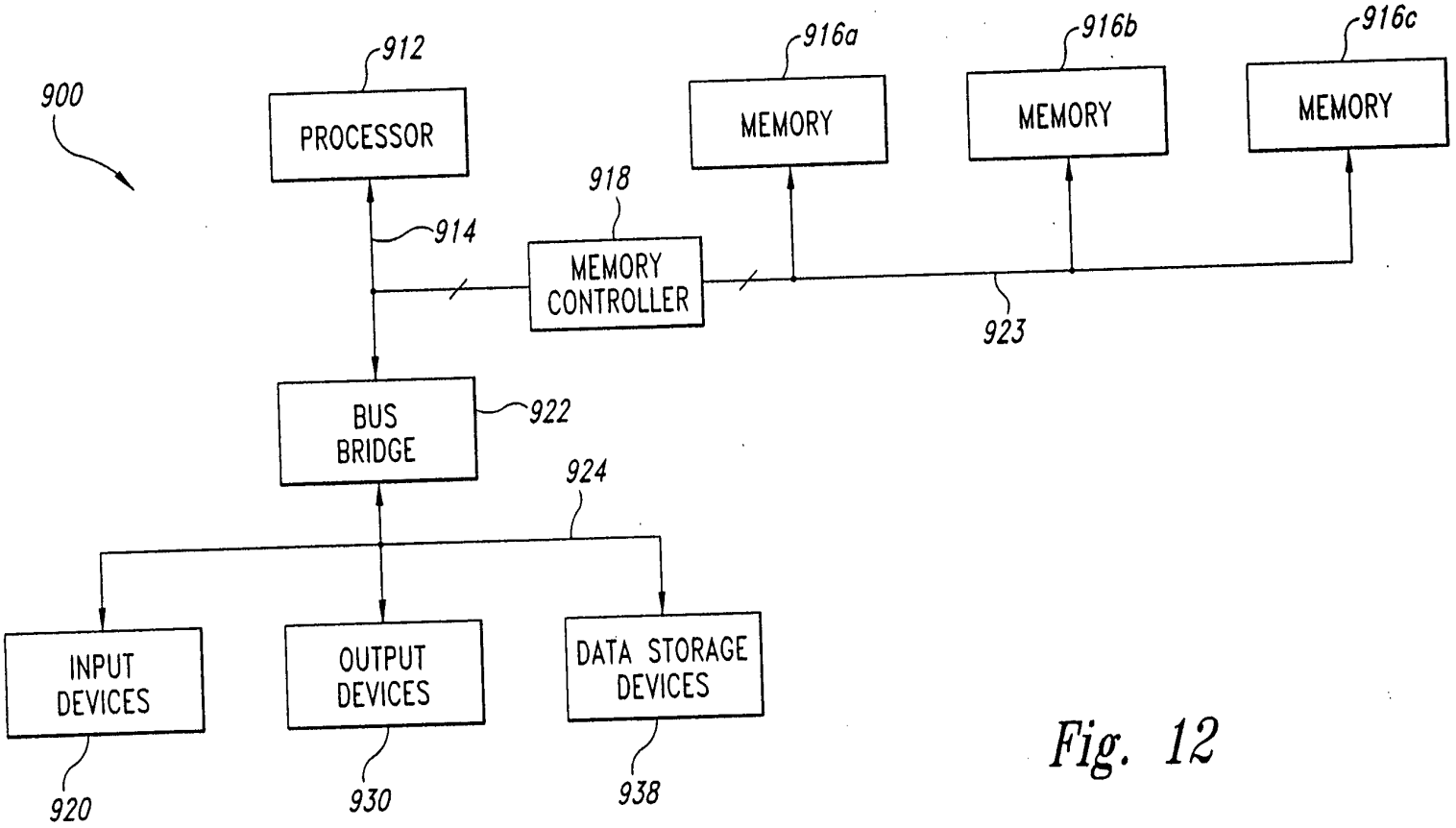

900
912
PROCESSOR
916a
MEMORY
916b
MEMORY
916c
MEMORY
918
914
MEMORY CONTROLLER
923
BUS BRIDGE
922
924
INPUT DEVICES
OUTPUT DEVICES
DATA STORAGE DEVICES
920
930
938

Fig. 12